AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double brackets indicating deletions.

Listing of the Claims:

1. (CURRENTLY AMENDED) A multi-chip semiconductor package comprising:

a plurality of stacked semiconductor package structures, each semiconductor package structure including;

a substrate having an upper surface and a lower surface;

a semiconductor chip mounted on the upper surface of the substrate, the semiconductor chip including an active surface and a backside surface;

an enclosure body covering substantially the entire upper surface of the substrate;

a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface; and

at least one conductive member formed in contact with the lower surface of at least one of the conductive studs.

2. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration;

wherein the at least one conductive member of the upper package structure is in electrical contact with at least one conductive stud of the lower package structure.

3. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration;

wherein the at least one conductive member of the upper package structure is in direct electrical contact with the at least one conductive member of the lower package structure.

4. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the substrate includes

a conductive layer, the conductive layer having an upper surface and a lower surface, and

an insulating layer, the insulating layer being formed on the lower surface on the conductive layer.

5. (ORIGINAL) A multi-chip semiconductor package according to claim 4, wherein:

the active surface of the semiconductor chip includes conductive pads, the conductive pads being electrically connected to the conductive layer.

6. (ORIGINAL) A multi-chip semiconductor package according to claim 5, wherein:

backside surface of the semiconductor chip is recessed below a plane defined by the upper surface of the conductive layer.

7. (ORIGINAL) A multi-chip semiconductor package according to claim 6, wherein:

the active surface of the semiconductor chip is substantially coplanar with or recessed below the plane defined by the upper surface of the conductive layer.

8. (ORIGINAL) A multi-chip semiconductor package according to claim 5, wherein:

conductive balls are formed on a plurality of bond pads on the active surface of each semiconductor chip, the conductive balls providing direct electrical contact to the conductive layer.

9. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the at least one conductive member includes a plurality of solder balls.

10. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the at least one conductive member includes a conductive pattern.

11. (ORIGINAL) A multi-chip semiconductor package according to claim 1, wherein:

the substrate includes conductive layer, the conductive layer having an upper surface and a lower surface, and an insulating layer formed on the upper surface of the conductive layer;

and further wherein

a second plurality of conductive studs extend through the insulating layer and are electrically connected to corresponding ones of the plurality of conductive studs extending through the enclosure body.

12. (CURRENTLY AMENDED) A multi-chip semiconductor package comprising:

an upper semiconductor package structure and a lower semiconductor package structure, each semiconductor package structure including;

a substrate having an upper surface and a lower surface and including a conductive layer and an insulating layer;

a semiconductor chip mounted on the upper surface of the substrate, the semiconductor chip including an active surface and a backside surface;

an enclosure body covering substantially the entire upper surface of the substrate;

a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface;

wherein at least one conductive member is formed in contact with the lower surface of at least one of the conductive studs of the upper semiconductor package structure; and

the upper semiconductor package structure and the lower semiconductor package structure are positioned so that the at least one conductive member is in electrical contact with the upper surface of at least one conductive stud of the lower semiconductor package structure.

13. (ORIGINAL) A multi-chip semiconductor package according to claim 12, wherein:

the at least one conductive member includes a plurality of solder balls formed on the lower surfaces of a plurality of the conductive studs of the upper semiconductor package structure; and

the plurality of solder balls are in electrical contact with the upper surfaces of corresponding conductive studs of the lower semiconductor package structure.

14. (ORIGINAL) A multi-chip semiconductor package according to claim 12, wherein:

the semiconductor chip is mounted in a recessed orientation in which the backside surface lies below a plane defined by the upper surface of the substrate.

15. (ORIGINAL) A multi-chip semiconductor package according to claim 12, wherein:

the insulating layer includes a resin material and the conductive layer includes a metallic material.

16. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package comprising:

providing a substrate, the substrate having an upper surface and a lower surface;

forming a plurality of conductive studs, the conductive studs extending through the substrate;

mounting a semiconductor chip on the upper surface of the substrate;

forming an enclosure body encapsulating the upper surface of the substrate, the semiconductor chip and the conductive studs;

removing an upper portion of the enclosure body to expose an upper surface of the conductive studs;

forming a conductive member on a portion of the lower surface of the substrate in electrical contact with the conductive studs to complete a semiconductor package structure; and

mounting a plurality of stacked semiconductor package structures so that the conductive member of an upper semiconductor package structure is in electrical contact with a lower semiconductor package structure.

17. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

the conductive member of the upper semiconductor package structure is in electrical contact with conductive studs of the lower semiconductor package structure.

18. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

the conductive member of the upper semiconductor package structure is in electrical contact with conductive member of the lower semiconductor package structure.

19. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

providing the substrate includes:

forming conductive layer, the conductive layer having an upper surface and a lower surface;

forming an insulating layer on the lower surface of the insulating layer; and

removing portions of the insulating layer, the removed portions corresponding to locations of the conductive studs.

20. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package according to claim 19, wherein:

the insulating layer is a resin layer; and

the portions of the insulating layer are removed after forming the conductive studs.

21. (ORIGINAL) A method of manufacturing a multi-chip semiconductor package according to claim 1 comprising:

forming the plurality of semiconductor package structures, each semiconductor package structure being formed by

preparing the substrate;

forming the plurality of conductive studs on the substrate, the conductive studs extending through the substrate;

mounting the semiconductor chip on the substrate;

forming electrical connections between the active surface of the semiconductor chip and the upper surface of the substrate on which the semiconductor chip is mounted;

forming the enclosure body encapsulating the upper surface of the substrate, the semiconductor chip, the electrical connections and the conductive studs;

removing an upper portion of the enclosure body to expose the upper surface of the conductive studs; and

forming the conductive member on the lower surface of the substrate, the conductive member being in electrical contact with the lower surface of at least one of the conductive studs; and

stacking an upper semiconductor package structure and a lower semiconductor package structure whereby the conductive member of the upper semiconductor package structure is in electrical contact with a corresponding conductive stud on the lower semiconductor package structure.

22. (NEW) A multi-chip semiconductor package according to claim 1, wherein the upper surface of the conductive studs extends to an upper surface of the enclosure body and the lower surface of the conductive studs extends to a lower surface of the enclosure body.

23. (NEW) A multi-chip semiconductor package according to claim 12, wherein the upper surface of the conductive studs extends to an upper surface of the enclosure body and the lower surface of the conductive studs extends to a lower surface of the enclosure body.

24. (NEW) A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein forming the plurality of conductive studs includes:

extending an upper surface of the conductive studs to an upper surface of the enclosure body; and

extending a lower surface of the conductive studs to a lower surface of the enclosure body.